AMENDMENTS TO THE CLAIMS

1. – 58. (Cancelled).

59. (Currently Amended) A processor system comprising:

a processor; and

memory device coupled to said processor, said processor and memory device residing on a [[common]] substrate, said substrate having a through-hole, said substrate further comprising a top side and a bottom side with a multi-layer structure provided [[interposed]] on both sides of said substrate and passing through said through-hole, said multi-layer structure comprising:

a conductive layer [[plane]]; [[and]]

a signal wiring layer, said conductive layer [[plane]] and said signal wiring layer having an insulating layer interposed between them; and

an interconnect wiring structure extending from said signal wiring layer through said insulating and conductive layers.

60. (Currently Amended) The processor system of claim 59, wherein said conductive layer [[plane]] comprises a first ground layer [[plane]].

61. (Currently Amended) The processor system of claim 60, wherein said first ground layer [[plane]] is at least 3 μm thick.

62. (Currently Amended) The processor system of claim 60, wherein the thickness of said first ground layer [[plane]] is less than or equal to 5 μm.

63. (Currently Amended) The processor system of claim 59, wherein said conductive layer [[plane]] comprises a power supply distribution layer [[plane]].

64. (Currently Amended) The processor system of claim 59, wherein said conductive layer [[plane]] comprises a copper layer [[plane]].

65. (Currently Amended) The processor system of claim 59, wherein said conductive layer [[plane]] comprises an aluminum layer [[plane]].

66. (Currently Amended) The processor system of claim 59, wherein said multi-layer structure further comprises a first insulating layer provided on the side of said multi-layer structure directly adjacent to said substrate.

67. (Original) The processor system of claim 66, wherein said first insulating layer comprises a silicon dioxide layer.

68. (Original) The processor system of claim 67, wherein the thickness of said silicon dioxide layer is 0.1 to 0.5μm.

69. (Currently Amended) The processor system of claim 66, wherein said conductive layer [[plane]] is deposited over said first insulating layer.

70. (Currently Amended) The processor system of claim 59, wherein said insulating layer comprises a second insulating layer formed over said conductive layer [[plane]].

71. (Original) The processor system of claim 59, wherein said multi-layer structure further comprises a third insulating layer formed over said signal wiring layer.

72. (Currently Amended) The processor system of claim 71, wherein said multi-layer structure further comprises a second conductive layer [[plane]] formed over said third insulating layer.

73. (Original) The processor system of claim 70, wherein said second insulating layer comprises silicon dioxide.

74. (Original) The processor system of claim 70, where the thickness of said second insulating is 0.5 to 4.0μm.

75. (Original) The processor system of claim 59, wherein said signal wiring layer comprises at least one signal line.

76. (Original) The processor system of claim 75, wherein said at least one signal line is 6 to 10 μm wide.

77. (Original) The processor system of claim 71, wherein said third insulating layer comprises a silicon dioxide layer.

78. (Currently Amended) The processor system of claim 72, wherein the thickness of said second conductive layer [[plane]] is 3 μm to 5 μm.

79. (Original) The processor system of claim 75, wherein said at least one signal line is terminated at a bond pad.

80. (Original) The processor system of claim 70, wherein said second insulating layer comprises a polyimide layer.

81. (Original) The processor system of claim 71, wherein said third insulating layer comprises a silicon dioxide layer.

82. (Original) The processor system of claim 71, wherein said third insulating layer comprises a polyimide layer.

83. (Currently Amended) The processor system of claim 72, wherein said second conductive layer [[plane]] comprises a ground layer [[plane]].

84. (Currently Amended) The processor system of claim 72, wherein said second conductive layer [[plane]] comprises a power supply distribution layer [[plane]].

85. (Currently Amended) The processor system of claim 72, wherein said multi-layer structure further comprises a fourth insulating layer formed over said second conductive layer [[plane]].

86. – 131. (Cancelled).

132. (New) A chip system comprising:

a substrate for mounting at least one chip, said substrate having at least one through-hole and at least one circuit component formed thereon;

a multi-layer structure covering both sides of said substrate and passing through said at least one through-hole, said multi-layer structure comprising at least one conductive layer and a signal wiring layer, said at least one conductive layer and said signal wiring layer having an insulating layer interposed between them; and

wherein said signal wiring layer has an interconnect wiring structure in electrical communication with said at least one circuit component, said interconnect wiring structure extending through said insulating and conductive layers.

133. (New) The chip system of claim 132, wherein said conductive layer comprises a first ground layer.

134. (New) The chip system of claim 133, wherein said first ground layer is at least 3 μm thick.

135. (New) The chip system of claim 133, wherein the thickness of said first ground layer is less than or equal to 5 μm.

136. (New) The chip system of claim 132, wherein said at least one conductive layer comprises a power supply distribution layer.

137. (New) The chip system of claim 132, wherein said at least one conductive layer comprises a copper layer.

138. (New) The chip system of claim 132, wherein said at least one conductive layer comprises an aluminum layer.

139. (New) The chip system of claim 132, wherein said multi-layer structure further comprises a first insulating layer provided on the side of said multi-layer structure directly adjacent to said substrate.

140. (New) The chip system of claim 139, wherein said first insulating layer comprises a silicon dioxide layer.

141. (New) The chip system of claim 140, wherein the thickness of said silicon dioxide layer is 0.1 to 0.5 μm.

142. (New) The chip system of claim 139, wherein said at least one conductive layer is deposited over said first insulating layer.

143. (New) The chip system of claim 132, wherein said insulating layer comprises a second insulating layer formed over said at least one conductive layer.

144. (New) The chip system of claim 143, wherein said second insulating layer comprises silicon dioxide.

145. (New) The chip system of claim 143, wherein the thickness of said second insulating layer is 0.5 to 4.0 μm.

146. (New) The chip system of claim 143, wherein said second insulating layer comprises a polyimide layer.

147. (New) The chip system of claim 132, wherein said multi-layer structure further comprises a third insulating layer formed over said signal wiring layer.

148. (New) The chip system of claim 147, wherein said multi-layer structure further comprises a second conductive layer formed over said third insulating layer.

149. (New) The chip system of claim 148, wherein the thickness of said second conductive layer is 3 μm to 5 μm.

150. (New) The chip system of claim 148, wherein said second conductive layer comprises a ground layer.

151. (New) The chip system of claim 148, wherein said second conductive layer comprises a power supply distribution layer.

152. (New) The chip system of claim 148, wherein said multi-layer structure further comprises a fourth insulating layer formed over said second conductive layer.

153. (New) The chip system of claim 147, wherein said third insulating layer comprises a silicon dioxide layer.

154. (New) The chip system of claim 147, wherein said third insulating layer comprises a silicon dioxide layer.

155. (New) The chip system of claim 147, wherein said third insulating layer comprises a polyimide layer.

156. (New) The chip system of claim 132, wherein said signal wiring layer comprises a second signal line.

157. (New) The chip system of claim 156, wherein said second signal line is 6 to 10 μm wide.